Characterization and application of selective all-wet metallization of silicon

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Received 29 August 2011, in final form 3 November 2011
Published 8 December 2011
Online at stacks.iop.org/JMM/22/015003

Abstract

We demonstrate selective, two-level metallization of silicon using electroless deposition of copper and gold. In this process, adhesion between the copper and silicon is improved with the formation of intermediary copper-silicide, and the gold layer protects copper from oxidation. The resistivity and residual stress of Au/Cu is 450 $\Omega\text{nm}$ (220 $\Omega\text{nm}$ annealed) and 56 MPa (tensile), respectively. These Au/Cu films allow a truly conformal and selective coating of high-aspect-ratio Si structures with good adhesion. We demonstrate the potential of these films in microswitches/relays, accelerometers and sensors by conformally coating the sidewalls of long (up to 1 mm in length), slender microbeams (5 $\mu\text{m} \times 5 \mu\text{m}$) without inducing curvature.

1. Introduction

Integration of metals with semiconductors has been a crucial milestone in shaping today’s integrated circuit and microsystem technologies [1–3]. There has been great interest, both economically and scientifically, to improve upon existing metallization schemes [2]. The replacement of Al-based interconnect technology with a Cu-based one in ultralarge-scale-integration (ULSI) technology is a good example of this trend. Among metallization processes, electrochemical methods have recently received particular attention due to certain unique advantages they offer—such as low film stress, ease of fabrication and low cost [2–4]. In this category, electroless deposition (ED) has also seen an increase in the number of applications, including in biomedical devices [5–7], micro-electro-mechanical systems (MEMS) [8–10], fuel cells [11, 12], ULSI [4, 13] and molecular nanodevices [14]. The primary advantages of ED include selective deposition without the need for electrical connections, as well as high-quality coatings that are uniform and conformal [1].

Galvanic displacement (GD; also known as immersion plating) can be considered a type of ED, although most researchers use the term ED to refer to autocatalytic plating processes [1, 15]. The main difference between autocatalytic plating and GD is that the former uses reducing agents in the solution to deposit metal ions on the substrate, whereas GD corrodes the underlying substrate to reduce the metal ions onto the substrate. This difference implies that the GD thin films would be relatively more porous due to the need for constant electron/ion exchange between the GD solution and the substrate [1]. GD is a self-limiting process, since access to the underlying substrate is blocked as the thickness of the deposited film goes up. Hence, the thickness range that can be achieved with this process is limited to hundreds of nanometers. The resulting adhesion between the metal and the semiconductor substrate is typically weak and needs to be improved with the deposition of a seed/buffer layer between the metal and the substrate or with the inclusion of different additives in the deposition solution [16]. The seed/buffer layer can be deposited via physical vapor deposition (PVD) methods [17] or electroless activation of the substrate surface directly [18]. However, PVD methods tend to compromise the conformal and selective nature of ED and may block the electron/ion exchange for GD. Hence, direct wet activation of the surface is the only current ED approach that results in a truly conformal and selective metallization scheme.

A variety of materials can be deposited using GD, such as Cu, Ni, Au, Pt and Ag. However, when exposed to air, active materials—such as Cu or Ni—form oxide layers that in some cases (including Cu) may advance through the entire thickness of the film [19]. One common approach to solve this problem is to cap these films using noble materials, such as Au. Electroless Ni immersion Au is frequently used by the industry for this purpose to cap thick Cu films. The electroless
Ni layer between Cu and Au in this process acts as a diffusion barrier to prevent out-diffusion of Cu through the Au layer. In this study, we apply the principles of ED to fabricate suspended micromechanical structures with conformal and selective metallization using Cu and Au. Electroless Au prevents Cu from oxidation for a reasonable amount of time (approximately 5 months at room temperature) until a hermetic packaging/assembly scheme can be adopted to increase the lifetime of fabricated devices. We improved Cu adhesion to Si with a simple Cu-silicide (Cu$_3$Si) formation step. Here, we demonstrate long (up to 1 mm in length) and slender (cross-sectional area of 5 × 5 μm) micro-cantilevers metalized conformally with Au/Cu without inducing any curvature. Although there have been previous attempts to combine ED and suspended MEMS devices for selective and conformal metallization of Si structures [9, 10], such studies feature only one level of metallization on relatively stiff mechanical transducers. Furthermore, unlike previous attempts, our silicon metallization precedes the dry release of suspended structures, which improves the quality of the thin film on Si and increases the fabrication yield. We have used simple curvature measurements on the metalized cantilevers to quantify the type and magnitude of thin film stress. We characterize additional thin film properties of the deposited Cu and Au/Cu layers through energy-dispersive x-ray spectroscopy (EDS), scanning-electron-microscopy (SEM) and four-point probe measurements.

2. Fabrication

2.1. GD of Cu on Si

GD of Cu uses Si as the reducing agent; therefore, the Si surface has to be cleaned thoroughly with hydrofluoric acid (HF; 10%) dip to remove any native oxide on Si. The plating solution is based on a formulation used by other researchers [9] and is comprised mainly of analytical grade copper sulfate (CuSO$_4$·5H$_2$O; 0.01 M) and ammonium fluoride (NH$_4$F; 20% vol). The solution also includes ascorbic acid (C$_6$H$_8$O$_6$; 0.015 M), sodium potassium tartrate (KNaC$_4$H$_4$O$_6$·4H$_2$O; 0.015 M), polyethylene glycol (PEG; 20 mL L$^{-1}$) and methanol (CH$_3$OH: 30% vol) to improve the film quality and reduce Cu on the Si surface at room temperature:

Anode : Si(s) + 6F$_{aq}^{-}$ → SiF$_{aq}^{2-}$ + 4e$^-$

E$^o$ = 1.2 V vs NHE

Cathode : Cu$_{aq}^{2+}$ + 2e$^-$ → Cu(s)

E$^o$ = 0.34 V vs NHE.

Here, aq and s represent the aqueous and solid phases, respectively. After getting uniform coverage of the entire exposed Si surface, rapid thermal annealing under a nitrogen environment at 400 °C for 10 min enables Cu to sinter with Si to form Cu-silicide (Cu$_3$Si) [20]. Non-reactive extra Cu on the surface agglomerates into small bulbs that would otherwise interfere with uniform deposition of subsequent layers. They can be removed using piranha solution (H$_2$SO$_4$·H$_2$O$_2$: 3:1, at around 85 °C) without affecting the underlying Cu-silicide that will act as an adhesion/buffer layer for the subsequent deposition of Cu and Au. The piranha solution removes/etches not only the elemental Cu residues but also any other organic contaminants as well, yielding a clean Cu-silicide surface. After this step, another Cu deposition is carried out on top of the existing Cu-silicide with a HF dip in between to remove any oxide on the surface. The second layer of Cu follows the same deposition mechanism as the first one with similar material properties and morphology.

2.2. Direct immersion gold

Since active Cu surface oxidizes rapidly, it needs to be capped immediately with a noble metal, such as Au. Direct immersion gold (DIG) is a relatively new approach that has been formulated to meet the industry’s need for defect-free surface finishes for second level interconnect technology [21]. The method uses a combination of GD and autocatalytic deposition to form relatively pore-free selective Au thin films on Cu. DIG initiates the Au deposition with GD on Cu and proceeds with autocatalytic deposition on top of the newly formed Au. The DIG method in our approach uses a cyanide-based formulation (from Uyemura, Ontario, CA) (equation (3)) with 20% GD and 80% autocatalytic deposition, with the reaction taking place at 85 °C and a pH value of 5.5:

\[
\text{Au(CN)}_2^+ + e^- \rightarrow \text{Au}_{(s)} + 2CN^- 
\]

(3)

2.3. Microfabrication of cantilevers

Cantilever fabrication is performed on the device layer (5 μm) of silicon-on-insulator (SOI) wafers with a buried oxide thickness of 2 μm and top oxide of 500 nm (figure 1(a)). The cantilever beams are patterned using standard lithographic processes and an anisotropic reactive ion etch (RIE) based on SF$_6$·C$_4$H$_8$ (figure 1(b)). The electroless Au/Cu layer is deposited selectively and conformally only on the sidewalls of the cantilever beam (figure 1(c)) as explained in sections (2.1) and (2.2). After the metal deposition is complete, a custom HF (49%) vapor system is used to release the cantilevers (figure 1(d)). HF vapor offers excellent selectivity against Si, Cu and Au/Cu with no detectable damage.

3. Results and discussion

GD of Cu produced smooth and shiny finishes on Si and passed the standard scotch-tape peel-off test with good reliability and yield. Inclusion of different additives as outlined in section (2.1) proved helpful in improving the film quality and the wettability of the solution. However, the Cu thin film lifted off when exposed to the DIG solution at 85 °C. Application of an intermediary Cu-silicide buffer layer solved this problem with no peel-off on the subsequent Cu thin film. We believe that this is a good indication of improved adhesion due to the formation of Cu-silicide. Thermal budget for the formation
Figure 1. (a) SOI wafer with a device layer of 5 μm, a buried oxide layer of 2 μm and a top layer of 500 nm. (b) Photolithography and RIE to etch/pattern device layer Si and top oxide layer. (c) Electroless Cu and Au deposition along the sidewalls. (d) HF (49%) vapor release.

Figure 2. (a) Digital picture of a Si piece plated with Cu. (b) EDS of the plated Cu on Si. (c) SEM of the plated Cu with a thickness of 170 nm on Si. (d) Digital picture of a Si piece plated with Au/Cu. (e) EDS of the plated Au/Cu on Si shows the incorporation of Au within the thin film. (f) SEM of the plated Au/Cu with a total thickness of 500 nm on Si. The scale bars depict 1 μm.

of Cu-silicide can be further optimized if high-temperature annealing is not desired. It is reported that Cu can sinter with Si at as low as 250 °C [20].

We used EDS and SEM to inspect the composition and quality of the deposited metal layers. Visually, there was a clear color difference between the Cu and Au/Cu films (figures 2(a) and (d)), and EDS confirmed the incorporation of Au within the latter (figures 2(b) and (e)). SEM was useful in visualizing the deposited layer profiles (figures 2(c) and (f)). We checked the deposition rate of Cu on both Si and Cu-silicide over a fixed exposed Si area (57 mm²) using the same volume of Cu solution (25 ml). As expected, the thickness showed saturation with time because access to the underlying silicon got hindered and the ion concentration in the solution was
Cu shows symmetric exponential behavior. The worst-case contribution of underlying silicon to these measurements has been estimated to be less than 5%. The measured resistivity values are about ten times higher than those reported for Cu or Au due to the additional conduction path through the 5 μm thick Au [19]. We believe that the high resistivity of the thin films deposited by traditional methods such as e-beam evaporation is due to the relatively porous nature of the thin films [1].

The decrease in resistivity after annealing is consistent with the type and the level of stresses on the plated thin films. The stress on the plated films was removed before the film deposition so the thin film could be less than 5%. The measured resistivity values are about ten times higher than those reported for Cu or Au thin films deposited by traditional methods such as e-beam evaporation [19]. We believe that the high resistivity of the films is due to the porous nature of the thin films [1].

Out-diffusion of Cu into Au has been an issue for solder joint reliability on Cu interconnect technologies [21]. Ni is currently used to prevent the diffusion between Cu and Au. However, the inclusion of Ni comes with certain drawbacks. For instance, it is necessary to precede Sn sensitization and Pd activation [8], and Ni causes problems for radio frequency electronics due to the ferromagnetic properties of Ni [25].

DIG finishes on Cu have been sought for the prevention of Cu out-diffusion through Au [21]. In our case, Cu diffusion time can be estimated by using the standard solution to Fick’s second law, assuming a fixed surface concentration of Cu with semi-infinite Au thickness [25]:

$$C(x, t) = \frac{C_i}{2} \left(1 - \text{erf}\left(\frac{x}{2\sqrt{Dt}}\right)\right),$$  \hspace{2cm} (4)

where x is the position through the thickness of Au (cm) starting at the Cu and Au interface, t denotes time (s), C is the concentration of Cu (mol cm⁻³) within the Au volume, Cᵢ is the surface concentration of Cu at the interface (mol cm⁻³), D is the diffusion constant for Cu within Au (cm² s⁻¹) and erf is the error function. Specifically, with a Cu diffusion constant of 10⁻¹⁹ (cm² s⁻¹) [21, 25] and a Au thickness (along the x-axis) of 50 nm, the solution gives approximately 5 months before 0.1% of the interface concentration of Cu is reached on the top surface of Au at room temperature. If a Hermetic sealing process is adopted within this timeframe, the lifetime of Au/Cu can be improved indefinitely without any exposure to the oxidizing environment. Any additional processing after the film deposition should account for the effect of temperature for the out-diffusion of Cu. For instance, at a temperature of 175 °C, the out-diffusion of Cu can be on the order of hours [21]. ED of Au/Cu in this fashion on suspended silicon structures is hence an attractive metallization option during the latter stages of fabrication that do not involve a high thermal budget.

We utilized radius of curvature measurements on the cantilever beams metalized with Cu and Au/Cu to estimate the type and the level of stresses on the plated thin films. The microfabrication of the test cantilever beams was conducted as explained in section (2.3) except that the top oxide layer was removed before the film deposition so the thin film could deposit on the top side as well (figure 4(a)). We used optical methods to measure the free-end deflection of the fabricated cantilevers (figure 4(b)) and Stoney’s equation to estimate the stress on the plated films [26]. We found that the plated Cu (100 nm) and Au/Cu (100 nm) films had tensile stresses with a magnitude of 45 and 56 MPa, respectively. After annealing at 150 °C for 30 min, the free-end deflections
Figure 4. (a) Cut-view of a metalized Si cantilever beam (5 μm × 5 μm) over the buried silicon dioxide (2 μm thick) before the release (scale bar: 1 μm, film thickness: 350 nm). (b) The free end of the metalized cantilever (1.1 mm long) released with HF vapor (scale bar: 10 μm, film thickness: 100 nm). (c) Cut-view of the Si on the buried oxide (2 μm thick) with only sidewall metallization (scale bar: 1 μm, film thickness: 100 nm). (d) The free end of a cantilever (1 mm long) with only sidewall metallization after HF vapor release (scale bar: 1 μm, film thickness: 100 nm).

went up, corresponding to the tensile stress increasing to 78 MPa for Cu and 130 MPa for Au/Cu. The increase in the radius of curvature can be attributed to the film structure changes, such as grain growth [24], or the increased adhesion between the thin film and Si due to the formation of additional Cu-silicide.

The microfabrication of cantilever beams with only sidewall deposition allowed for straight metalized, slender cantilevers (5 μm × 5 μm) up to 1 mm in length (figures 4(c) and (d)). The main failure mechanism was the occasional stiction of the beams to the handle layer of the SOI wafer during the HF vapor release step. We believe that one could get longer beams with even smaller cross-sectional areas by using different Si (device layer) and buried-oxide layer thicknesses.

4. Conclusion

In summary, we report the application and characterization of all-wet metallization of Si using the electroless deposition of Cu and Au. The interface between Si and Cu has been improved with a simple formation of intermediary Cu-silicide layer such that the subsequent Au deposition does not cause any peel-off on the plated Cu. We estimate that Au protects Cu for quite a reasonable amount of time, so a Hermetic packaging scheme can be adopted. We have applied the selective and conformal nature of the electroless deposition to fabricate very long (up to 1 mm in length), slender (5 μm × 5 μm) metalized micro-cantilever beams with a very simple, one-mask fabrication process.

We expect that the long, high-aspect-ratio micro-machined structures metalized with such a simple process sequence can help achieve reduced cost and high yield in the realization of a wide variety of electro-mechanical transducers, including capacitive sensors, accelerometers, RF elements and microrelays/switches. Furthermore, the ability to realize highly compliant, metalized mechanical structures without stress imbalance issues may enable a dramatic reduction in actuation voltages of such transducers. Finally, rapid and selective metallization of silicon nanodevice arrays in this manner could facilitate easy bio-functionalization of their active surfaces through the standard Au chemistries at reduced cost and labor. As such, the electroless Au/Cu deposition process we describe here may be useful in the realization of practical biosensors, as well.

Acknowledgments

The authors gratefully acknowledge the support from NSF (grant no ECCS-0601630) and the ONR (grant no N00014-09-01-0197). We thank Bozidar Marinkovic for help in testing and characterization.
References


